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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,395	11/26/2001	Sergey D. Lopatin	039153-0457 (G1162)	7882

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,395	LOPATIN ET AL.	
	Examin r	Art Unit	
	Thomas J. Magee	2811	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11032003* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. There are a number of objections based on informalities contained within the claims. These include the following: a) Claims 3 and 4 – there is no mention of a *"characteristic for lowering resistivity"* referred to in either Claim 1 or 2, b) Claim 5 --- there is no mention of a *"lowered resistivity"* in either Claim 1 or 2, and c) Claims 12 and 13 --- there is no mention of a *"characteristic for lowering resistance,"* in either Claim 10 or 11. Correction is required.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obvious-ness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 6,030,895) in view of Edelstein et al. (US 6,399,496 B1), Harper et al. (US 5,243,222), and Cunningham ("Improving Copper Interconnects: A Search for Useful Dopants," Semiconductor International, April, 2000, pp. 1 – 8).

4. Regarding Claims 1 – 3, Joshi et al. disclose a method for fabricating an interconnection structure used on a device in an integrated circuit wherein a barrier layer (34,40) (Figure 2) (Col. 4, lines 50 – 62) is formed along the lateral sidewalls and bottom of a via aperture, where the via aperture is configured to receive a via material that connects a first and second conductive layer. Joshi et al. further disclose that the via material is subsequently deposited (Col. 8, lines 5 – 8) and comprises a ternary Cu alloy (Col. 8, lines 24 – 27). Edelstein et al. disclose that the ternary alloy (Col. 8, lines 49 – 52) can be formed using Cu, Zn (Col. 8, lines 42 – 45) and Cr (Col. 8, lines 35 – 41) and formed in a via. Further, Edelstein et al. disclose that a ternary alloy (Col. 8, lines 49 – 52) can be formed comprising the following: CuAgCr (Col 8, lines 35 – 45) and CuSnCa (Col. 8, lines 31 – 41). Harper et al. disclose that alloying element additions of less than one atomic percent Cr are used in producing Cu alloy interconnect structures (plugs) that exhibit high current density tolerances (Col. 6, lines 2 – 14). Cunningham discloses that in electrochemically deposited (plated) alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious to combine Edelstein et al., Cunningham and Harper et al. with Joshi et al. to obtain stable Cu alloy regions that exhibit large grains from alloy element additions, thereby increasing current carrying capacity and resistance to electromigration.

5. Regarding Claims 4 and 5, Joshi et al. do not disclose that Zn or Ag in concentrations of one atomic percent or less can alter resistivity. However, Cunningham discloses (Figure 4) that additions of Zn or Ag can change the resistivity of copper (1.9 uOhm-cm) From Figure 4, the altered resistivity is approximately in the range, 1.6 to 1.75 uOhm-cm. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Cunningham with Joshi et al. to obtain low resistance Cu alloy conductive regions.

6. Regarding Claims 2 and 3, Joshi et al. do not explicitly disclose that the resistance is lowered with copper alloys, but Andricacos et al. disclose (Col. 8, lines 43 – 54) that low resistivity (resistance) is obtained with ternary copper alloys containing In, C, or Sn. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Anricacos et al. with Joshi et al. to obtain low resistance Cu alloy conductive regions.

7. Regarding Claims 4 and 5, Joshi et al. do not disclose that the element is contained in the alloy at levels of one atomic percent or less, or the value of the lowered resistivity. Andricacos et al. disclose (Col. 8, Table 1) that the resistivity of copper alloys containing one percent or less of Sn and other alloying elements is in the range, 1.9 to 3.1 micro-ohm-cm, which is in the range recited in the instant application. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the Andricacos et al. in Joshi et al. to produce Cu multi-element alloys of varying resistivity and to combine Andricacos et al., with Joshi et al.

8. Regarding Claims 6 – 9, Joshi et al. do not disclose the effect of alloying elements on grain size. Harper et al. disclose that alloying element additions of less than one atomic percent Cr are used in producing Cu alloy interconnect structures (plugs) that exhibit high current density tolerances (Col. 6, lines 2 – 14). Cunningham discloses that in electro-chemically deposited (plated) alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious to combine Cunningham and Harper et al. with Edelstein et al. to obtain stable Cu alloy regions that exhibit large grains from alloy element additions, thereby increasing current carrying capacity and resistance to electromigration.

9. Claims 10 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. in view of Andricacos et al. (US 6,090,710).

10. Regarding Claims 10 – 13, Joshi et al. disclose a method of using a ternary copper alloy (Col. 8, lines 24 – 27) to obtain interconnect or via structures in which a first conductive layer (M1) (Figure 2) is provided over an integrated circuit substrate, followed by the formation of a conformal layer at the bottom and sides of a via aperture to form a barrier layer separating the via from the first conductive layer. Further, Joshi et al. disclose that the via aperture is filled with copper alloy to form a ternary via and a second conductive layer (M2) formed over the via, electrically connecting first and second conductive layers.

Edelstein et al. do not explicitly disclose that the addition of select alloying elements will yield low resistance within the copper vias. However, Andricacos et al. disclose (Col. 8, Table 1) that the resistivity of copper alloys containing one percent or less of Sn (>98% Cu) and other alloying elements is altered. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Andricacos et al. with Joshi et al. to obtain low resistance (resistivity) copper alloys for vias. (resistance). In addition, Cunningham discloses that in alloyed layers subsequent to annealing, the "doped" (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious at the time of the invention to one of ordinary skill in the art to combine Cunningham with Edelstein et al. to obtain ternary alloy vias of low resistance and large grain size to improve reliability and improve resistance to electromigration.

11. Claims 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. in view of Cunningham, as applied to Claim 10, and further in view of Harper et al.

12. Regarding Claims 14 – 16, Joshi et al. do not disclose the effect of alloying elements on grain size. Harper et al. disclose that alloying element additions of less than one atomic percent Cr are used in producing Cu alloy interconnect structures (plugs) that exhibit high current density tolerances (Col. 6, lines 2 – 14). Cunningham discloses that in alloyed layers subse- quent to annealing, the "doped" (alloyed) material

exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. It would have then been obvious to combine Cunningham and Harper et al. with Edelstein et al et al., to obtain stable Cu alloy regions that exhibit large grains from alloy element additions, thereby increasing current carrying capacity and resistance to electromigration.

13. Claims 17 - 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. in view of Edelstein et al.

14. Regarding Claims 17 and 19, Joshi et al. disclose a method of forming a via in an integrated circuit, wherein a first conductive layer (M1) (Figure 2) is formed, followed by deposition of

an etch stop layer (34) over the first conductive layer and an insulating layer (14) over the etch stop layer, whereupon, an etch is applied and an aperture formed in the insulating layer and etch stop layer. Joshi et al. further disclose that a barrier material (40,34) is provided at the bottom and sides of the aperture, followed by a fill of the aperture with a ternary (Col. 8, lines 24 – 27) Cu alloy and formation of a second conducting line (M2), where the via electrically connects the first and second conductive layers. Joshi et al. do not disclose the constituents of the Cu alloy. Edelstein et al. disclose that a ternary alloy (Col.8, lines 49 – 52) can be formed using Cu, Zn (Col. 8, lines 42 – 45) and Cr (Col. 8, lines 35 – 41) and formed in a via. It would have been obvious to one of ordinary skill in

the art at the invention to use the procedures of Edelstein et al. in Joshi et al. to obtain a filled via with a combination of improved electromigration resistance, adhesion, and surface properties (Edelstein et al., Col. 8, lines 51 – 52)

15. Regarding Claims 18 and 20, Joshi et al. do not disclose a copper alloy material that includes Cu, Sn, and Ca or that the compound source includes CuAgCr and CuSnCa. Edelstein et al. disclose that a ternary copper alloy (Col. 8, lines 49 – 52) can be formed Comprising the following: CuAgCr (Col.8, lines 35 – 45) and CuSnCa (Col. 8, lines 31 – 41). It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the ternary alloy of Edelstein et al. in Joshi et al. to obtain a filled via with a combination of electromigration resistance, adhesion, and surface properties (Edelstein et al., Col. 8, lines 51 – 52).

16. Claims 21 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al., in view of Edelstein et al. as applied to Claims 17 – 20 above, and further in view of Cunningham.

17. Regarding Claims 21 – 23, Joshi et al. do not disclose the effect of alloying elements on grain size or the stuffing of grain boundaries. Cunningham discloses that in deposited alloyed layers subsequent to annealing, the “doped” (alloyed) material exhibits growth of grains to a size of 1 - 5um (page 3, 1st paragraph) with columnar structure. Cunningham further discloses that within the copper alloy, precipitation of elements and compound

formation occurs at the grain boundaries (page 5, 1st paragraph). It would have then been obvious to combine Cunningham with Edelstein et al. to obtain copper alloys with large grains and localized precipitation at grain boundaries to increase resistance to electromigration.

Response to Arguments

18. Applicant's arguments with regard to claim rejections have been carefully considered but these are rendered moot in terms of the new grounds of rejection. However, a few comments should be made. Examiner does not agree with Applicant's assertion that the references cannot be combined. It is the formation of a workable alloy approach that is "combined" with primary references to obtain an alloy with increased grain size and altered resistivity. Examiner also does not agree with Applicant's characterization of the Cunningham reference, in regard to dopants. Figure 4 clearly shows the effect on resistivity. Additionally, the influence on grains is disclosed, reading on the limitations of the instant application. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusions

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
January 28, 2004

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